UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,168,024 B2
APPLICATION NO. : 10/678625
DATED : January 23, 2007
INVENTOR(S) : Farnsworth

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On The Title Page,

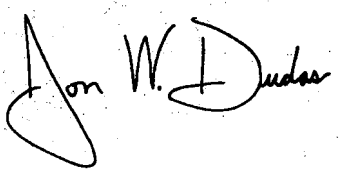
Item [57]: ABSTRACT should read: --A method for generating at least one error checking code includes creating a modified input data word, including (k+m) bits, by combining an input data word, having n-bits, with at least a previously calculated at least one error checking code, including m-bits, where $n \leq k$, and calculating a first m-bit error checking code from at least a first selected portion of the modified input data word. --

Column 13,

Line 10: Should read: --code, comprising m-bits, where $n \leq k$, and --

Signed and Sealed this

Thirtieth Day of October, 2007



JON W. DUDAS
Director of the United States Patent and Trademark Office